REMARKS

Prior to examination of the above-identified application, please enter this preliminary amendment, amending claims 8, 11, 13, and 17, and adding new claims 20 – 29. No new matter has been added. Applicant respectfully requests an action on the merits.

Respectfully submitted,

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APPENDIX

Claims 8, 11, 13, 17 have been amended at pages 18 – 23, as follows. Claims 20 –29 have been added at page 23, line 22, as follows:

IN THE CLAIMS:

8. (Amended) A method for at least two-bit equalization of an input signal to compensate for a channel frequency response, comprising:

generating a delayed input signal;

generating at least two intermediate output signals to identify if and when adjustments need to be made to the input signal;

converting the delayed input signal and the at least two intermediate output signals to a differential delayed input signal and at least two differential intermediate output signals;

selecting an equalization step size for each of the at least two intermediate output signals based on the channel frequency response;

dividing a tail current into at least three weighted current segments based on the equalization step size;

inputting the differential delayed input signal, the at least two differential intermediate output signals, and the at least three weighted current segments into at least three differential [pairs] amplifiers that output at least three output currents; and

combining the at least three output currents to form an equalized output signal.

11. (Amended) A two-bit equalization system to output an equalized signal

compensated for a channel frequency response, comprising:

a decision subsystem to decide when an input signal is adjusted and to output a delayed input signal and two output signals, the decision subsystem having

a delay module to align the input signal with the two output signals,

an exclusive-or (XOR) circuit, an inverted exclusive-or (XNOR) circuit, and a delay module to output a first output signal,

a XOR circuit, an [or] OR circuit, and a XNOR circuit to output a second output signal; and

an equalization subsystem to output the equalized signal compensated for a channel frequency response having

a tail current switch to direct a tail current,

a plurality of current control bits to partition the tail current into three branches with an amount of each current predetermined by selected control bits, and

three differential [pairs] amplifiers to accept as input the partitioned tail current branches, the delayed input signal, the first output signal, and the second output signal from the decision subsystem, and to output three currents that are combined to form the equalized signal.

13. (Amended) A transmitting device to send an input signal on a channel, comprising:

an equalization system to perform at least a two-bit equalization, including:

a decision subsystem to decide when an input signal is adjusted and to

output a delayed input signal and at least two output signals, the decision subsystem having:

a delay module to align the input signal with the two output signals,

an exclusive-or (XOR) circuit, an inverted exclusive-or (XNOR) circuit, and a delay module to output a first output signal,

a XOR circuit, an [or] OR circuit, and a XNOR circuit to output a second output signal; and

an equalization subsystem to produce an equalized output signal compensated for a channel frequency response having:

a tail current switch to direct a tail current,

a plurality of current control bits to partition the tail current into three branches with an amount of each current predetermined by selected control bits, and

at least three differential [pairs] amplifiers to accept as input the partitioned tail current branches and the delayed input signal, the first output signal, and the second output signal from the decision subsystem, and to output three currents that are combined to form the equalized output signal; and

a transmitter to send the equalized output signal as the input signal to the channel.

17. (Amended) A machine readable storage medium, comprising:

machine-readable program code, stored on the machine readable storage medium, the machine-readable program code having instructions to

generate a delayed input signal;

generate at least two intermediate output signals to identify if and when adjustments need to be made to the input signal;

convert the delayed input signal and the at least two intermediate output signals to a differential delayed input signal and at least two differential intermediate output signals;

select[ing] an equalization step size for each of the at least two intermediate output signals based on the channel frequency response;

divid[ing]e a tail current into at least three weighted current segments based on the equalization step size;

input the differential delayed input signal, the at least two differential intermediate output signals, and the at least three weighted current segments into at least three differential [pairs] amplifiers that output at least three output currents; and

combine the at least three output currents to form an equalized output signal.

20. (New) A method for transmit equalization of an input signal, comprising:

selecting at least two equalization step sizes;

dividing a tail current into at least three weighted current segments based on the at least two equalization step sizes;

inputting a differential delayed input signal into a differential amplifier and inputting at least two differential intermediate output signals into at least two additional differential amplifiers;

inputting the at least three weighted current segments into the differential amplifier and the at least two additional differential amplifiers to output at least three output currents; and

combining the at least three output currents to form an equalized output signal.

21. (New) The method of claim 20, wherein a delayed input signal and at least two intermediate output signals [were] are converted to form a differential delayed input signal and the at least two differential intermediate output signals.

22. (New) The method of claim 20, wherein the at least two intermediate output signals determine if and when adjustments are to be made to the input signal.

23. (New) The method of claim 20, wherein weight of the weighted current segments is determined either by default or by user, by a plurality of control bits in a control subsystem.

24. (New) The method of claim 20, wherein the number of control bits is six.

25. (New) A transmitting device, comprising:

an equalization step selection subsystem to select equalization step adjustment sizes to adapt to a channel characteristic and to transmit the equalization step sizes;

an equalization subsystem to receive the equalization step sizes, a delayed input signal, and at least two intermediate output signals, to apply the equalization step adjustment sizes to the at least two intermediate output signals, and to produce an equalized output signal compensated for the channel characteristic; and

a transmitter to send the equalized output signal to a channel.

26. (New) The transmitting device of claim 25, wherein the channel characteristic is the channel frequency response.

27. (New) The transmitting device of claim 25, wherein the channel is a copper wire channel.

28. (New) The transmitting device of claim 25, wherein the channel is a printed circuit board trace.

29. (New) The transmitting device of claim 25, wherein the channel is an optical fiber channel.